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Removing Barriers to All-Wet Single-Wafer Cleans in Packaging-Related Applications

Kimberly D. Pollard, Richard Peters, Travis Acra, Don Pfettscher, Josh Cummins, Diane Scheele, [Dynaloy LLC]
Spencer Hochstetler, Peter Shang, San Sutanto, [Eastman Chemical Company]
Thorsten Matthias, Thomas Glinsner, Martin Schmidbauer, [EV Group]

The use of negative dry film or negative spin-on film photoresist has been very common in semiconductor packaging processes. Film thicknesses ranging from 10µm to 120µm have been incorporated into processes ranging from redistribution to solder bump application. Removal of these films at rates reasonable for manufacturing processes has always been challenging, usually requiring 1) processes that are between 20 and 120min in length, or 2) a plasma gas-based etch process followed by a wet clean to complete. A process flow diagram is shown in **Figure 1.**

As a result of requirements for these process flows, immersion cleaning developed so that multiple wafers, typically 25 to 50 at a time, could be processed simultaneously and increase the tool throughput while still accommodating the long process time. The success with this type of processing allowed thick negative films to be successfully incorporated throughout the packaging process. However, this solution to increase throughput, although providing a more reasonable cost-of-ownership (CoO), has been accommodated by trade-offs in other areas of the overall process.

As wafer feature dimensions continue to be scaled down, the trade-offs have a greater and greater impact on the process. For example, when batch immersion processes are run, the photoresist strip solution is reused to clean multiple batches, using a standard unchanging recipe defining the process time and temperature, solution recirculation rates, rinse solutions, etc. The best photoresist removal solution (chemistry) to match the static process conditions would be a static strip solution in which the composition would not vary, despite the number of cleaning processes that had been done. Practically, this condition cannot be met with an immersion process. Photoresist removal solutions behave differently throughout their lifetime due to 1) resist being dissolved in them, which can change further resist dissolution rates, possibly requiring extended clean times; 2) evaporation at the operation temperature, which changes component concentration and can affect cleaning efficiency or compatibility characteristics; 3) consumed reactive components that can create concentration changes leading to less effective stripping performance or changing compatibility with permanent materials on the wafer surface; 4) undissolved resist build up that provides a continuously growing source of particles; and 5) surface finish of the wafer after the strip process, which, if altered, may require additional processing to be integrated into the packaging process. Additionally, the traditionally long process times for batch immersion clean processes create additional challenges when rework is necessary.

Long processes provide extended contact of strong chemical solution with the wafer surface. Even solutions that have an etch rate for a permanent material, for example Cu, that is in the range of 5Å/min, will lose ~450Å in a 90-minute process. If that wafer was processed in a strip solution that has a non-linear Cu etch rate as a function of process time and/or solution lifetime, then more Cu could be lost. If re-work is required, then an additional process will be necessary. In the above example, ~1000Å of Cu could be lost, possibly exceeding the maximum allowable loss specification. In addition, even if the Cu loss is within process guidelines, it may be removed from the surface unevenly, thereby creating integration issues as the wafer moves to subsequent processes.

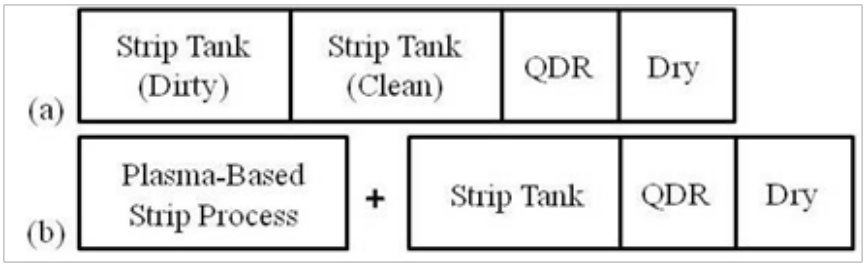


Figure 1: Process flow diagram. **a)** batch immersion strip process, **b)** plasma plus batch post-etch residue removal process

Reducing Variability

All the issues discussed above describe opportunities for reducing variability in production cleans processes, which is a source of yield loss. The goal of this paper is to discuss a new technology that can improve on the trade-offs while maintaining a competitive CoO. Combining the capability to develop wet chemical resist removal solutions with an understanding of process and tool requirements has led to the development of a single-wafer cleaning technology for photoresist removal. This technology targets the existing and developing needs in wafer-level packaging: removing thick cross-linked films such as photoresists and fluxes, while maintaining the pre-clean integrity of the solder bump, exposed metals, and dielectrics. The platform, called CoatsClean™, enables the manipulation of chemistry to a degree that allows for significantly reduced chemical usage and short process times in a single bowl tool. In addition to environmental sustainability, the reduced chemical usage allows the use of fresh, unused solution on every wafer leading to improved wafer-to-wafer consistency and a CoO that can be lower than other immersion or single-wafer tool processes. This technology platform provides flexibility in cleaning processes including the ability to balance resist removal with materials compatibility, increased stability of chemical formulations, increased formulation possibilities, and the ability to run multiple wafer types and chemistries on the same tool.

Figure 2 shows images of a variety of electroplated solder bumped 200mm and 300mm wafers cleaned using the new technology, consisting of the EVG301RS tool, resist strip solution, and process. The optical images illustrate cleaning results after the removal of thick resist and again after the subsequent field metal etch process, indicating that the surface is finished in a manner that can be integrated into the next process step. Additionally, the scanning electron microscope (SEM) images show a more detailed view of compatibility with the solder bump and Cu field metal surface after the photoresist removal step.

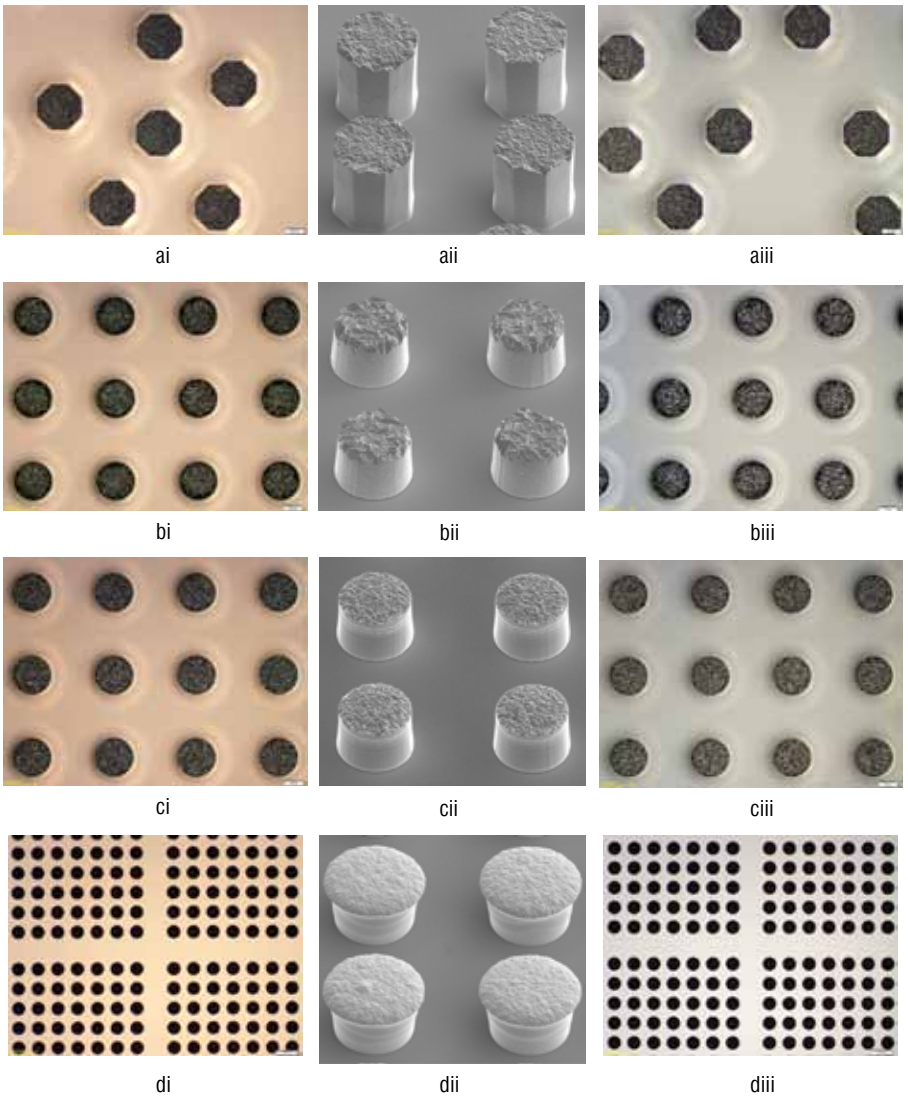


Figure 2: Images i) optical, after resist strip, ii) SEM, after resist strip, iii) optical after field metal etch. a) Resist removed 120µm TOK 50120, solder, SnAg; b) Resist removed 80µm Asahi Sunfort CX8040, solder SnAg; c) Resist removed 80µm Asahi CX8040, solder Cu pillar, LF cap; d) Resist removed, 55µm AZ4620, solder eutectic

CoO Considerations

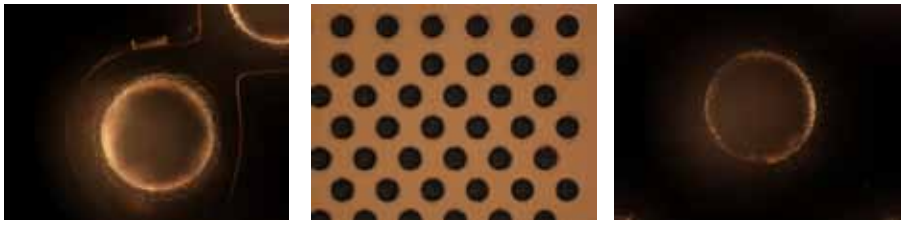
As discussed previously, CoO was a large driver in the development of batch immersion processes for thick resist removal. This is particularly true for negative tone resists because additional cross-linking occurs during exposure, making the polymer more challenging to remove, especially when

Step 1	Step 2	Step 3
Low volume of room temp. CoatsClean solution dispensed onto wafer surface	Solution rapidly heated to activation temperature. Resist is stripped	Rinsed with water and dried in a single bowl

Figure 3: a) Process flow in a CoatsClean™ tool

(a)

(b) (c) (d)



(e) (f) (g)

Figure 4: Optical images of a batch of dummy wafers, cleaned with different process conditions. **a**) unprocessed wafer; **b**) wafer processed in fresh typical resist strip solution, 60°C, 30min, front of cassette; completely clean **c**) wafer processed in fresh typical resist strip solution, 60°C, 30min, middle of cassette; showing residue **d**) wafer processed at end-of-resist-loading in a typical resist strip solution, 60°C, 30min, showing residue remaining where there was none for the same test in a fresh solution; **e**) dark field of bump area for image shown in d); **f**) wafer processed at end-of-resist-loading in a typical resist strip solution, 60°C, 60min, showing time required to complete cleaning of the surface; **g**) dark field image of bump area for image shown in f)

simultaneous compatibility with other wafer materials is required. In the past, single-wafer process tools and processes were considered an uneconomical choice because of the long process time (20–120min) and large volume of resist stripping solution (often > 1L) to process a single wafer. **Figure 3** shows a process flow for wafers cleaned using the new technology. 300mm wafers are processed using substantially reduced volumes of solution per wafer to remove resist in a single bowl, single-wafer clean process and using 3-10min (dry-dry) process times including processes to remove thick negative resists.

Optical images depicting the change in cleaning time as a function of wafer position and resist loading in the solution for a batch immersion process are shown in **Figure 4**. A process recipe is developed in which a process time is selected to be the same throughout the bath lifetime. Even if the fresh solution removes the resist more quickly, the wafer will remain in the solution for the same period of time as the last set of wafers cleaned in that solution. This may lead to process variability because the cleaned wafer surface in the first case is exposed to the hot reactive strip solution for a longer period of time than the last set of wafers. Another example of this variability shown in **Figure 4** is found when clean results are compared between wafers cleaned at the front of the cassette in the batch and those in the middle or the end. Fluid flow across the wafer surface is more restricted in the middle of the cassette than it is for the front wafer, typically removing the resist from the front of the wafer more quickly.

To provide further insight into the chemical changes that occur in photoresist strip solutions during the entire lifetime of the solution, an estimation of evaporation rate of dimethylsulfoxide (DMSO), at a common strip temperature of 60°C, was made. DMSO is a common solvent present in many photoresist stripping solutions. The thermal gravimetric analysis (TGA) is shown in **Figure 5**. From the plot, the evaporation rate of DMSO was calculated as 2%/min. This rate is considered an upper limit of the rate of evaporation because of the high surface to volume ratio. Additionally, in a photoresist removal solution, other components modify the evaporation rate, decreasing it from that reported in the figure. With surface area to volume ratios and air flow across the surface, etc., being equal, a 100% DMSO resist strip solution would be evaporated completely through a 12hr operation period. In practical terms, the evaporation rate is not that high but still significant. It is common practice to replenish resist removal solutions during the lifetime of the solution so batch levels do not get too low. Between evaporation of solvent and replenishment of solution through the course of the bath lifetime, there are changes in the resist strip formulation component ratios, changing the balance between the critical components. This change in balance may result in changing the solubility of resist, or it may change the effect of the solution on the exposed wafer surface.

The increase of particles in solution as multiple batches of wafers are processed is shown in the graph in **Figure 6**. When fresh solution is used for each cleaning step, the dissolving capability of the resist strip solution is

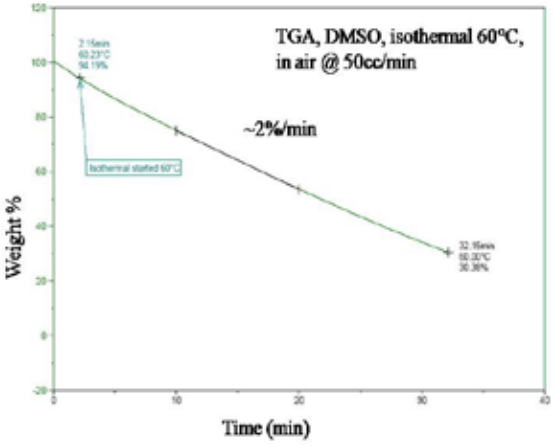


Figure 5: Thermal gravimetric analysis of DMSO. The evaporation rate can be calculated based on this experiment and illustrates that evaporation of even high boiling point solvents, such as DMSO, can affect the resist strip solution composition.

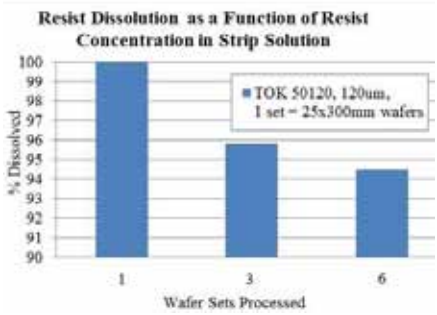


Figure 6: Resist dissolution, measured using particle analysis before and after resist strip of one set of wafers showing decreased dissolution and therefore increased numbers of particles in solution.

at a maximum, allowing for greatest dissolution. Maximum dissolution decreases the possibility of particles in solution redepositing onto the wafer surface and causing yield issues or requiring rework processes.

The continued increase in importance of wafer surface finish after cleans was predicted years ago and was described as being one of the next key challenges for the industry to address.[1] The challenge was tied to continued device shrinkage, and because scaling has continued, the prediction has been realized. An example of the increasing importance of the wafer surface finish has been found in lead-free solder bumping processes. It has been shown[2] that electroplated lead-free solder bumped wafers that have been stripped of photoresist show an increased probability of yield issues in the subsequent field metal etch process, even when they pass inspection. As a result, many line engineers have developed strategies to overcome the problems by changing the post-strip surface finish. The short process times of the tool discussed above offer an opportunity to have a surface finish that can be integrated with the field metal etch process step.

Summary

The advantages of a single-wafer tool that utilizes relatively small volumes of stripping solutions for thick resist removal were discussed in combination with the justification from a CoO perspective. The multidisciplinary approach effectively couples the chemistry for resist removal, the wafer clean process and the tool platform simultaneously, to deliver a flexible single bowl clean process. Cleaning and etch results from bumped 200mm and 300mm wafers with up to 120µm-thick negative dry film using a new single-wafer clean tool and process were demonstrated.

References

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2. K. Pollard, A. Rector, N. Wheeler, Chip Scale Review, Jan-Feb 2011, V15(1), pp. 22-26.

Contact Author

Kimberly D. Pollard, Technology Manager, Dynaloy LLC, a subsidiary of Eastman Chemical Company; email kimpollard@dynaloy.com

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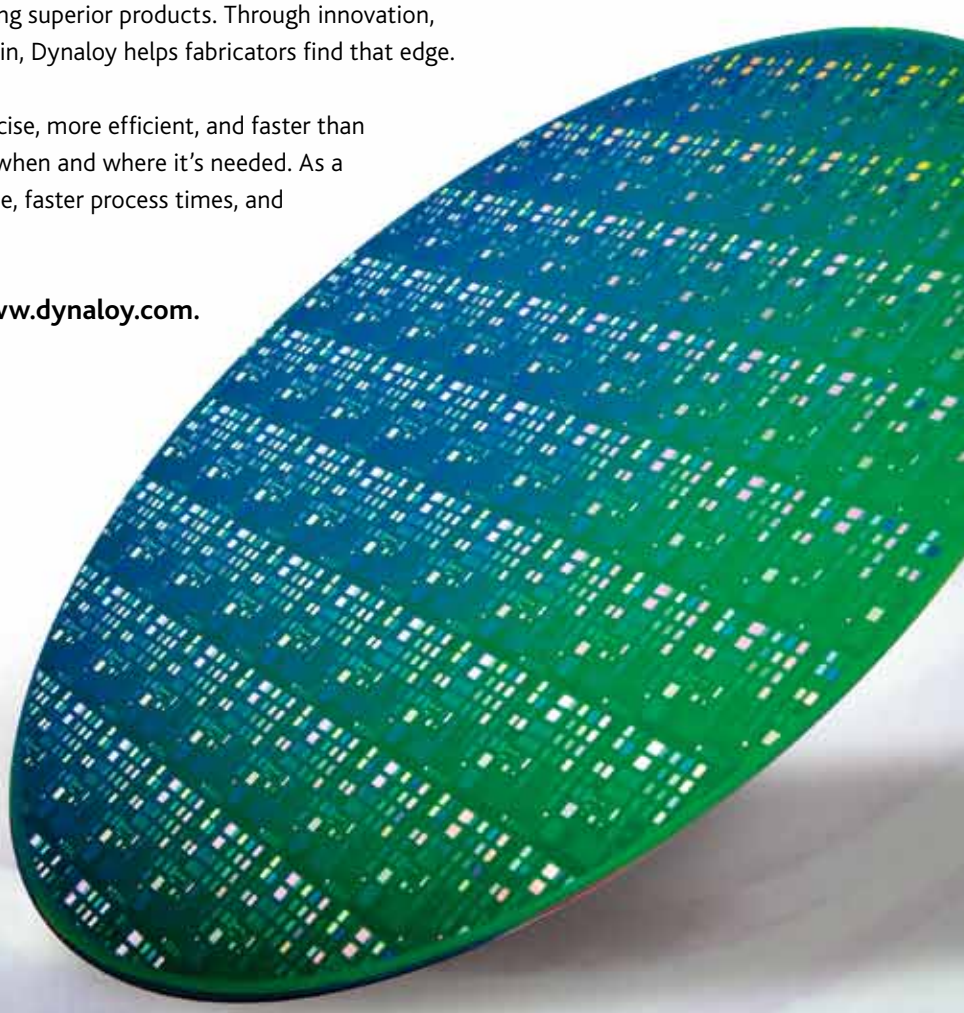

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